ABSTRACT OF THE DISCLOSURE

An apparatus in a pipeline microprocessor is provided that enables the microprocessor to execute programs written in native instructions to be executed directly from memory, This feature is provided in addition to the conventional capability of executing programs written using macro instructions that conform to a particular instruction set architecture. The apparatus includes instruction translation logic and bypass logic. The instruction translation logic typically retrieves macro instructions from memory that are provided via an external instruction bus. The instruction translation logic decodes each of the macro instructions into associated native instructions for execution by the microprocessor. The bypass logic is coupled to the instruction translation logic. When a special bypass macro instruction is executed, the bypass logic disables the instruction translation logic, and retrieves the native instructions directly from memory for execution by the microprocessor, thereby bypassing the instruction translation logic.